Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DONALD EUGENE DENNING,
ROBERT GEORGE EMBERTY,
and CRAIG ANTHONY KLEIN

Appeal No. 2002-1859
Application 09/131,846[1]

ON BRIEF

Before BARRETT, GROSS, and LEVY, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-18.

We affirm.

[1] Application for patent filed July 24, 1998, entitled "Data Processing Method and System for Simulation of Hardware Faults Utilizing a PCI Bus."

BACKGROUND

The invention relates to a method and system in a data processing system for simulating a hardware fault for a peripheral component interconnect (PCI) bus.

Claim 1 is reproduced below.

> 1. A method in a data processing system for simulating a hardware fault occurring on an expansion card, said expansion card coupled to a processing unit in said system utilizing a bus, said method comprising the steps of:
>
> specifying said hardware fault to simulate;
>
> determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card;
>
> creating an analog voltage signal representative of said specified hardware fault; and
>
> outputting said analog voltage signal during operation of said expansion card, wherein said hardware fault occurring on said expansion card is simulated.

The examiner relies on the following reference:

Gates	5,701,409	December 23, 1997

Claims 1-18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gates.

We refer to the final rejection (Paper No. 6) (pages referred to as "FR__") and the examiner's answer (Paper No. 12) (pages referred to as "EA__") for a statement of the examiner's rejection, and to the brief (Paper No. 11) (pages referred to as "Br__") for a statement of appellants' arguments thereagainst.

OPINION

Gates discloses an integrated circuit with a built-in bus error generation circuit for simulating a hardware fault on a PCI bus. During test, an error command (Fig. 7) is loaded into a command register of the bus error generation circuit via the bus terminals (abstract; col. 6, lines 10-20 & 60-64). The bus error generation circuit then decodes the command and either generates or simulates an error condition on the bus during a subsequent bus cycle (abstract). Status configuration registers are then read to determine whether the integrated circuit and other devices properly detected and/or handled the generated or simulated error (abstract; summary). The generated and simulated error condition commands cause incorrect parity values to be output onto the parity bus terminal to simulate one of several different error conditions on the PCI bus (e.g., col. 4, lines 32-42), such as a "Master Address Parity Error" (MADRSPARERR), "Master Write Data Parity Error" (MWDATAPARERR), or a "Target Data Parity Error" (TRDATAPARRERR).

We read claim 1 onto Gates as follows: "specifying said hardware fault to simulate" reads on loading an error command into the command register; "determining a signal to output utilizing said bus to simulate said hardware fault occurring on said expansion card" reads on decoding the error command to indicate an incorrect parity value, where the simulated "hardware

fault" is one of several parity errors; "creating an analog voltage signal representative of said specified hardware fault" reads on the voltage indicative of the incorrect parity value (e.g., output from XOR gate 109 in Fig. 3); and "outputting said analog voltage signal during operation of said expansion card, wherein said hardware fault occurring on said expansion card is simulated" reads on outputting the incorrect parity value onto the parity terminal of the PCI bus.

Appellants argue that their circuit includes a digital-to-analog converter 30 which generates "an analog voltage signal representative of said specified hardware fault ..." which is thereafter output during operation of the expansion card (Br5). It is argued that each of the claims recites utilization of analog voltages. The examiner states that "all voltage in common practice is analog" (FR2) and that the claims do not recite an analog-to-digital converter (EA4). Appellants note that "analog" is defined as "[p]ertaining to or being a device or signal having the property of continuously varying in strength or quantity, such as voltage or audio," whereas "digital" is defined as "in computing, analogous to binary because the computers familiar to most people process information coded as combination of binary digits (bits)." The examiner responds that since both appellant and Gates use the same PCI architecture, it is unclear how the physical properties of voltage on the bus line can differ (EA4).

We agree with the examiner that the voltage signals in Gates can be considered analog. The difference between analog and digital voltage signals is how the information is encoded. With analog signals, the information is carried in the magnitude of the voltage. With digital signals, two ranges of voltage are interpreted to correspond to one of two logical binary values (0 or 1) of information. Digital signals are analog voltages signals which are interpreted to correspond to logical 0s and 1s. In the real world, 0s and 1s are represented by a range of voltage values, not single values, and the signal may take on any value during a transition between a 0 and 1, or vice versa, a characteristic of analog signals; it is only when the signal has stabilized that it is interpreted to be a 0 or 1. While it possible that appellants' digital-to-analog converter (DAC) could produce more than two levels of output voltage, claim 1 does not call for a DAC or for any number of levels of output voltage. In fact, it appears that the claimed "analog voltage signal representative of said specified hardware fault" could be exactly the incorrect parity value voltage signal disclosed in Gates, which is interpreted as a digital signal. The disclosure does not describe the output values of the DAC. If the "analog voltage signal" in appellants' system can be interpreted as a digital signal, then appellants should not be arguing that there is a difference over Gates. It seems to us that appellants'

invention may be the use of a DAC to generate the voltage signal representative of a hardware fault, as opposed to the use of logic gates (such as XOR gate 109 in Fig. 3) in Gates. However, the examiner correctly noted that a DAC is not claimed. If it was, the examiner would then have tried to find prior art to show the obviousness of using a DAC in place of a logic gate.

Appellants argue (Br5):

> Further, even assuming for arguendo that all voltage is analog, nothing within Gates shows or suggests in any way the creation of an analog signal which is "representative of said specific hardware fault" as set forth within the claims of the present Application. The mere presence of the voltage level within Gates which does not constitute a logical "one" or "zero" fails to anticipate, show or suggest in any way the creation of an analog voltage signal which is representative of the specified hardware fault as expressly required by the present claims.

The examiner responds that Gates simulates a specific type of hardware fault, a parity error, which signals are placed on the bus by actual voltages (EA4-5). It is argued the logical "ones" and "zeros" are manifested by analog voltage signals on a PCI bus (EA5).

We agree with the examiner that the incorrect parity value output to the PCI bus (e.g., the output of XOR 109 in Fig. 3) is representative of a specific hardware fault: incorrect parity. The output is considered an analog voltage signal for the reasons already discussed. Appellants do not describe what hardware faults are represented by their "analog voltage signal." If the "analog voltage signal" in appellants' system can be interpreted

as a digital signal as in Gates, and we find no description that it cannot, then appellants should not be arguing that there is a difference over Gates.

For the reasons stated above we conclude that the examiner has established a prima facie case of anticipation which has not been rebutted by appellants. The rejection of claims 1-18 is sustained.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

LEE E. BARRETT
Administrative Patent Judge

ANITA PELLMAN GROSS
Administrative Patent Judge

STUART S. LEVY
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

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